WHAT IS CLAIMED IS:

1. A process of manufacturing a semiconductor feature for use in a semiconductor device, comprising:

forming an opening in a substrate through a patterned photoresist layer and a hardmask layer located over said substrate with a plasma;

trimming said photoresist layer with a plasma to create an exposed portion of said hardmask layer;

removing said exposed portion with a plasma to create a trench guide opening; and

creating a trench through said trench guide opening with a plasma.

2. The process as recited in Claim 1 wherein forming said opening includes patterning an opening through a bottom anti-reflective coating (BARC) layer located between said photoresist and said hardmask layer and a pad oxide located between said substrate and said hardmask layer.

3. The process as recited in Claim 1 wherein said hardmask layer is a silicon nitride layer.

4. The process as recited in Claim 1 wherein said forming,

said trimming, said creating, and said removing are conducted in a same plasma tool.

5. The process as recited in Claim 1 further including forming an oxide liner in said trench.

6. The process as recited in Claim 5 furthering including depositing an oxide in said trench to form an isolation structure.

7. The process as recited in Claim 6 further including removing said hardmask subsequent to forming said isolation structure.

8. The process as recited in Claim 1 wherein said trimming includes trimming with a plasma having a source power ranging from about 300 watts to about 700 watts, a bias power ranging from about 0 watts to about 150 watts.

9. The process as recited in Claim 8 wherein said trimming includes using gases including HBr, O_2, and Ar and a flow rate of each of said gases ranges from about 20 sccm to about 80 sccm.

10. The process as recited in Claim 1 wherein creating said trench includes forming said trench adjacent an active region of

said substrate.

11. A process of manufacturing an integrated circuit, comprising:

forming an isolation structure on a substrate adjacent an active region of said substrate, including:

forming an opening in a substrate through a patterned photoresist layer and a hardmask layer located over said substrate with plasma;

trimming said photoresist layer with a plasma to create an exposed portion of said hardmask layer;

removing said exposed portion with a plasma to create a trench guide opening; and

creating a trench through said trench guide opening with a plasma;

forming transistors on said active region; and

forming interconnects in dielectric layers located over said transistors, said interconnects interconnecting said transistors to form an operative integrated circuit.

12. The process as recited in Claim 11 wherein forming said opening includes patterning an opening through a bottom anti-reflective coating (BARC) layer located between said photoresist and said hardmask layer and a pad oxide located between said substrate and said hardmask layer.

13. The process as recited in Claim 11 wherein said hardmask layer is a silicon nitride layer.

14. The process as recited in Claim 11 wherein said forming an opening, said trimming, said creating, and said removing are conducted in a same plasma tool.

15. The process as recited in Claim 11 further including forming an oxide liner in said trench.

16. The process as recited in Claim 15 furthering including depositing an oxide in said trench to form said isolation structure.

17. The process as recited in Claim 16 further including removing said hardmask subsequent to forming said isolation structure.

18. The process as recited in Claim 11 wherein said trimming includes trimming with a plasma having a source power ranging from about 300 watts to about 700 watts, a bias power ranging from about 0 watts to about 150 watts.

19. The process as recited in Claim 18 wherein said trimming

includes including HBr, O_2, and Ar and a flow rate of each of said gases ranges from about 20 sccm to about 80 sccm.

20. The process as recited in Claim 1 wherein forming said transistors includes forming wells and source and drain regions in said active region.